IOSR Journal of Engineering (IOSR JEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
PP 27-31

Analysis of PLL circuit for Single Event Transient

Mahalaxmi Palinje
(Department of Electronics and Telecommunication Engineering, Atharva College of Engineering,Mumbai University, India)

Abstract: *Space exploration provides us with valuable information about the universe. Progress in this held is based upon understanding and solving number of issues. Radiation experienced by aircraft in the outer space is one of them, where the sun is the main source of radiation. Electronic components on board the aircrafts/spacecraft are exposed to these radiations which can cause reduction in the lifetime of a craft and even mission failure. Phase-locked loops (PLLs) are an integral part of many electronic systems. They are used for a number of applications such as local oscillator (LO) in wireless communication systems, clock recovery circuitry at the serial or parallel high speed data links, synchronizing data transmission and as a frequency synthesizer in digital systems. This report summarizes effects of radiation which is introduced in a phase locked loop circuit in the form of a current pulse.*

I. Introduction

Hazardous impact of radiation onto semiconductor devices/circuits/systems is one of the important concerns in space applications such as spacecrafts and airplanes. Semiconductor's deviation from normal states due to radiation can be classified into two categories: single event effect (SEE) and total induced dose (TID). SEEs are caused by penetration of highly energetic particles like heavy ions, which upset logic states of transistors in digital circuits; while TIDs represent semiconductor components' behaviours under long term exposure to radiation, including threshold voltage degradation, mobility degradation, and larger leakage current.

This work focuses on designing radiation hard phase-locked loops (PLLs) that can be employed as accurate and robust high frequency clock generators in space applications. [3] [4][5]SEE has instant effects on the logic states of frequency dividers and phase/frequency detectors in the PLLs. Also, an "SEE hit" might change the voltage level at the output of charge-pump or loop filter and would lead to erroneous output for a certain period of time or completely throw the PLL out of lock. TID may drift the threshold voltages or mobility and leakage currents in voltage controlled oscillators (VCOs), level shifters, and buffers, which could eventually cause the PLL to malfunction. Therefore, special design must be carried out to achieve radiation hard PLLs. The tuning range of the our circuit is 2.5 GHz for the VCO as we get good sinusoidal waveform up to this frequency range and in PHz we get slightly distorted sinusoidal waveform on our 45nm technology the tuning range improves if we further use more reduced technology like 35nm.

II. Phase Lock Loop

A Phase Locked Loop (PLL) is a closed-loop feedback control system that generates an output signal in close relation with the phase and frequency of an input "reference" signal. Also a phase-locked loop able to track an input frequency or it can generate a frequency that is a multiple of the input frequency. Thus, in steady-state, the difference between the input and output phases should not be changing over time; that is, the output phase of the PLL should be in lock" with the phase of the input reference signal.[1][2]

Charge Pump Phase Locked Loop : The block diagram showing operating principle of PLL is given in figure1.

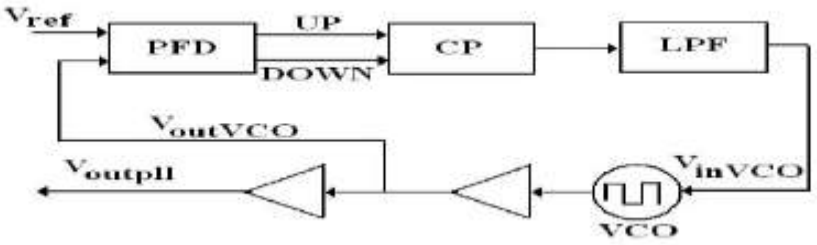

Figure 1: Functional block diagram of typical charge pump PLL [1]

Phase Frequency Detector (PFD) : The phase frequency detector in a phase-locked loop circuit generates a difference signal which is function of the phase difference (phase error) between the feedback signal to that of the input reference signal.

Charge Pump and Low Pass Filter : A Voltage Charge Pump can improve the speed of the acquisition since the current is not limited to a fixed value set by current sources, provided the values of the resistors of the LPF are chosen appropriately.

Voltage Controlled Oscillator and Buffers : The The output frequency of the VCO is directly proportional to the input dc level. The VCO frequency is adjusted till it becomes equal to the frequency of the input signal. During this adjustment, PLL goes through three stages free running, capture and phase lock..We are getting the lock state in the given transient time of 200ns for following operating frequency where lowest operating frequency is 250 MHz and highest operating frequency is 450 MHz.

III. Single Event Transient

Single event effect (SEE) in integrated circuits (IC) results in undesirable signal structure called single-event transient (SET). Recent works in PLLs show that mixed- signal circuits are particularly sensitive to Single-event transient. Single-event transient (SET) occurs when the charge collected from an ionization event discharges in the form of a spurious signal travelling through the circuit.The extra collected charge will cause a disruption of nodal voltages and may affect normal circuit operation. [1][6][7] Heavy ion strike due to radiation is the main reason for generation of SET in an electronic circuitry. When radiation strike occurs, SET propagates through the subsystem and reaches a circuit node where it can trigger a change. The charge pump stage, which supplies the current to the loop filter in a typical charge pump PLL, is the most sensitive stage with respect to SEE strikes. The vulnerabilities of PLL circuits due to single-event effect are of particular concern for space-systems, as SETs can result in errors within the IC. The vulnerability of a PLL is studied depending on the sub-circuit subjected to the ion strike. [9][10]

IV. Simulations and Results

A PLL is designed using 130nm process parameters. The simulation of the PLL circuit is done using circuit simulator HSPICE-2007 and then the waveforms are analyzed on waveform analyzer CosmoScope Ver.4 by Synopsys and finally the results are plotted. To study the effect of single-event transients on PLL circuit, a current source is introduced at the specific node in the PLL circuit which will have the same effect on circuit as that of a heavy-ion or a laser strike which produces SET effect in electronic circuitry. Therefore in circuit simulation, the charge deposition at a particular node in a circuit where radiation hit occurs is shown by a current source.

Simulation Environment :Pulsed model is used for the input reference signal data with pulse width of 10nsec 5 along with following time periods,Period = 20nsec,Pulse width = 10nsec. The current spikes are generated using an exponential function. A current source with 20mA value is used to produce the radiation effect and is as shown in fig. 2. A current source has been inserted at the output of charge pump-low pass filter and input to the voltage-controlled oscillator block i.e. Vinvco node of the complete PLL circuit and analyzed its effect on the PLL circuit. The current pulse is struck at the node Vinvco, which is the radiation vulnerable node in charge pump PLL circuit topology. The current spike is generated using an exponential function with pulsed value of 20mA at 20nsec and observed the initial changes in the output response. The total charge deposited due to 20 mA current pulse incident at the Vinvco node in charge pump-low pass filter circuit is 1.8045Pc

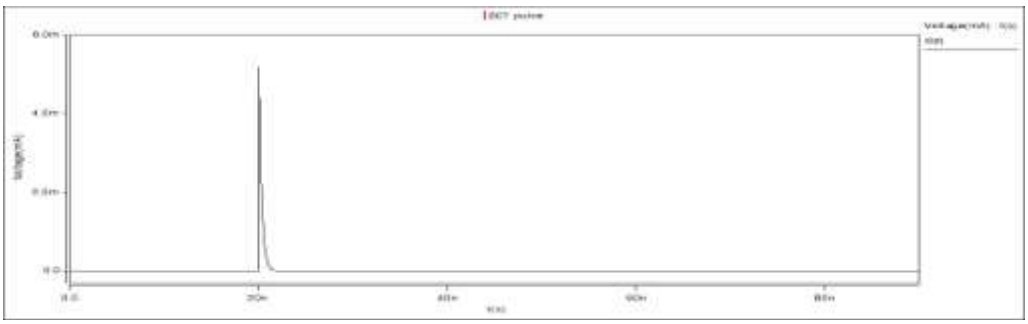

Figure 2: Current spike generated by transient source of 20mA

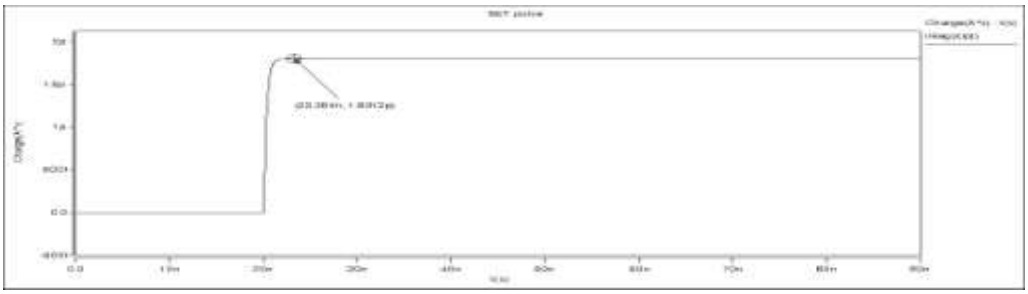

Figure 3: The total charge Q induced due to incident current pulse

Table 1: Amount of charge induced by Current spike of varying amplitude at the critical node

Amplitude of current pulse	Charge induced
80mA	7.3pC
60mA	5.5pC
40mA	3.7pC
30mA	2.8pC
20mA	1.8pC
15mA	1.3pC

Effects of radiation on PFD : There is certain delay in the locking of input reference frequency and Voutvco due to which there is distortion in the up and down output of phase frequency detector.

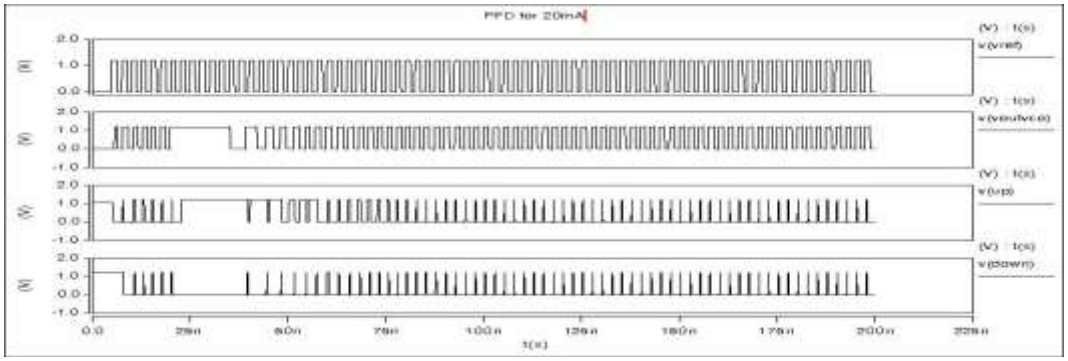

Figure 4: Simulation result for PFD block with SE strike of 20mA at 20nsec on Vinvconode.

Effects of radiation on CP-LPF : Strikes in the CP sub-circuit deposit/deplete charge to/from the capacitive load in the loop filter, thus adjusting the input voltage to the VCO. The frequency perturbation at the output of the VCO is therefore directly proportional to the change in stored charge in the loop filter. The output Vinvco, which would be high without the spike as shown in fig. 5, undergoes a negative transition but retains its original value after a specific amount of time period. This is illustrated in fig. 6

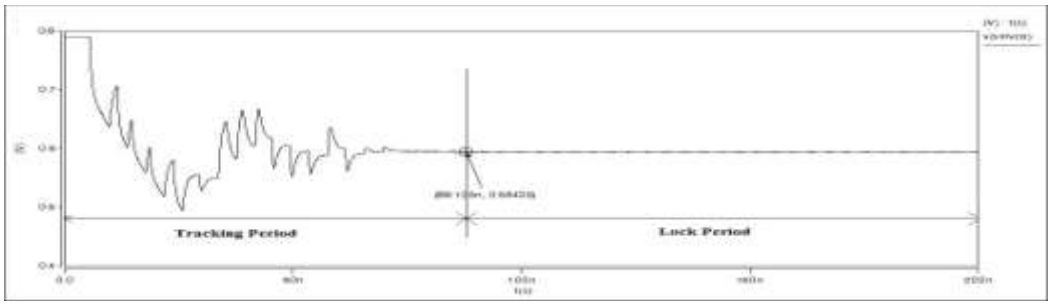

Figure 5: The output of CP-LPF, Vinvco vs time

The output Vinvco takes some time called tracking period to become stable implying that reference input signal Vdata is now in lock with feedback signal Vdclock. To study the effect of current pulse strike at Vinvco node a 20mA pulse is made incident at Vinvco at 20nsec and time taken to achieve stable position is recorded. The output Vinvco under the effect of current pulse regains its value within short time period and Vinvco remains constant indefinitely after 89.047nsec as PLL is in lock state now. Fig. 7 shows comparative

waveforms for Vinvco when current pulse of 20mA is inserted at 20nsec w.r.t. waveform without current pulse strike. Finally table below shows the effect of SE strike on Vinvco node when current pulse of different amplitudes is incident on Vinvco node in CP-LPF.

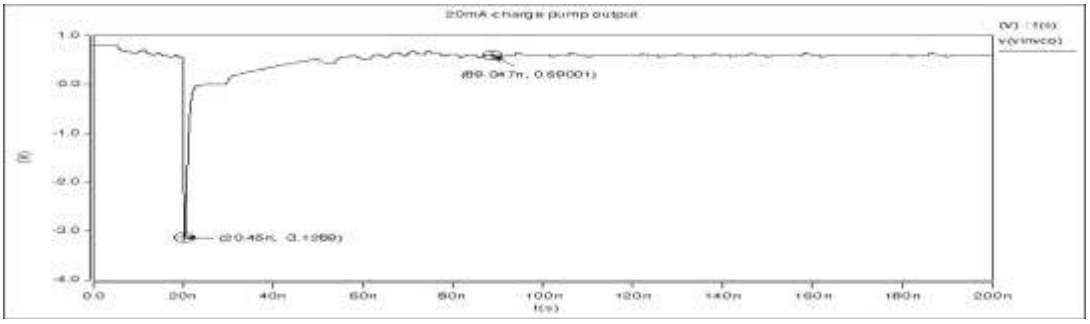

Figure 6: The output Vinvco due to 20mA current pulse incident at 20nsec

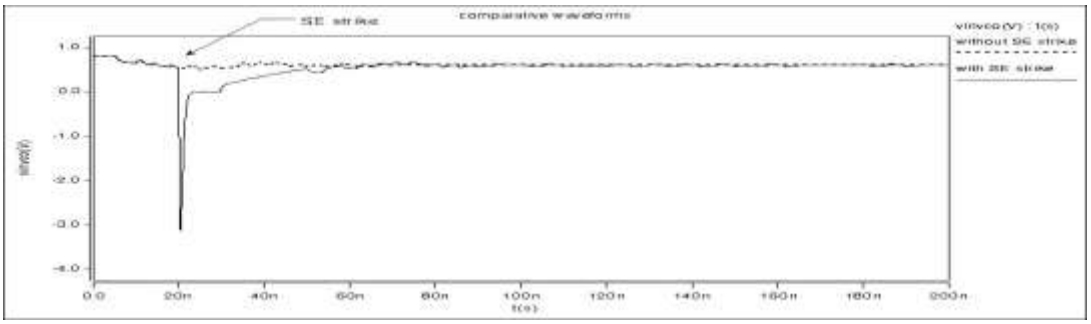

Figure 7: Comparative waveforms for Acquisition and lock curve: Vinvco Vs time.

Table 2: Comparative study of effect of SE strike with different amplitudes on Vinvco Node.

	Amplitude of Vinvco before strike (V)	Tracking period (Lock achieved at) (sec)	Time taken to recover from radiation effect (sec)	Amplitude of penetration (V)
No SE strike	-	76.45ns	-	-
20mA	0.55	89.04ns	69.04ns	-3.012
40mA	0.55	107.55ns	87.55ns	-6.4069
60mA	0.55	115.87ns	95.87ns	-10.465

Effect of radiation on: VCO: Figure 14 shows the simulation result of voltage controlled oscillator block under normal operating mode. From the figure below signal Vinvco attain stable condition 75.498nsec onwards. That is the reference input Vdata and feedback signal Vdclock achieves lock condition 75.498nsec onwards. Figure 15 shows simulation result for the PLL under radiation effect. A current source with amplitude 20mA (ISEU = 20mA) is inserted at 20nsec at output node of CP-LPF block. This causes output signal of oscillator i.e. Vclock to shift by 17.67nsec at 20nsec because of additional current introduced as a radiation. Fig 9 shows Vclock pulse simulated under the effect of radiation when current pulse of 20mA, 40mA and 60mA is incident at Vinvco node. From the figure it can be observed that Vclock pulse attain stability 94.05nsec onwards under the effect of 20mA current pulse strike, 107.9nsec onwards when 40mA current pulse strike, and 116.95nsec onwards when 60mA current pulse strikes PLL.

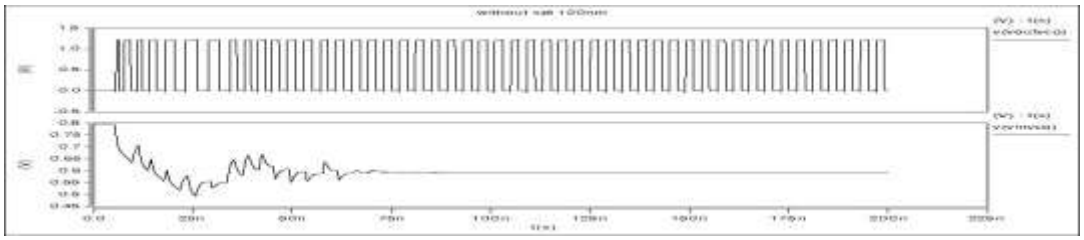

Figure 8: Simulation result for VCO block without SE strike.

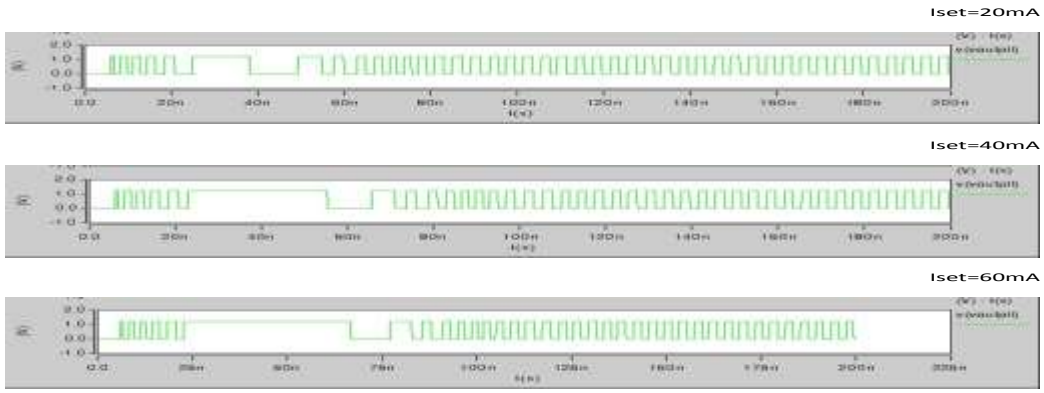

Fig: Simulation result for Voutpll signal with SE strike of 20mA, 40mA & 60mA at 20nsec

.

Figure9: Vclock pulse simulated under the effect of radiation when current pulse of 20mA, 40mA and 60mA is incident at Vinvco node

Table 3: Comparative study of effect of SE strike on Voutpll with different amplitudes of current pulses.

Current Strike at 20nsec at Vin-vco node					
Sr.No.	Voutpll	No strike	20mA	40mA	60mA
1	Pulse extended upto (from 20ns)	-	72.68ns	86.829ns	96.526ns
2	Pulse width (before radiation)	-	7.76ns	7.76ns	7.76ns
3	Pulse width (after radiation)	-	17.67ns	34.54ns	46.109ns
4	Lock achieved at	75.498ns	94.05ns	107.9ns	116.95ns
5	Amplitude of penetration (V)	-	-3.012	-6.4069	-10.465

V. Conclusion

The effects of SETs on a mixed-signal phase-locked loop have been analyzed. This analysis was performed using 130nm process parameter model file. Simulations are carried out by inserting a current pulse of magnitude 20mA, 40mA and 60mA at a circuit node, which will have the same effect on circuit as that of a heavy-ion or a laser strike which produces SET effect in electronic circuitry and finally results are tabulated and compared. The effects of single-event in each of the PLL blocks are analysed where charge pump-LPF block showing more vulnerability to the single event effects. As the amplitude of current pulse increases the control voltage applied as an input to the VCO decreases. The control voltage takes some time to regain its original amplitude level as that of before the current pulse was introduced. Simulation results shows more the amplitude of current pulse larger the time taken by PLL to achieve the lock condition. Thus PLL take more time to attain its original position disturbed by the current strike Also it is observed that as the total charge deposited by the current pulse strike (single-event) increases, the settling time also increases because the settling time is directly proportional to the amount of charge deposited at the circuit node. The radiation effects are also analysed for VCO block. For VCO block when 20mA current pulse was introduced at Vinvco node the lock was achieved at 94.05nsec. The results are observed for 40mA as well as 60mA current pulses and simulation results shows that the time taken by the Vinvco wave to attain its lost phase is decreased.

References

[1]. Utkarsh Gupta. Aunnasha Sengupta. Nachiket Nanadikar, Kapil Majumdar and S S Rathod, " Design of voltage charge pump Phase Locked Loop (PLL)", 2nd International Conference on global technology initiative, March 2013
[2]. B.Razavi , " Design of Analog CMOS Integrated circuit". McGraw-Hill International Edition.
[3]. Surendra Singh Rathod , A.K Saxena, Sudeb Dasgupta, " Radiation Effects in MOS based Device and Circuits : A Review" , IETE Technical Review, Vol-28, Issue-6, Nov-Dec2011
[4]. A.N Nemmani, "Design Techniques for Radiation Hardened Phase Locked Loop", (Master of Science, Thesis Paper)
[5]. Sung-Mo Kang,Yusuf Leblebici, "CMOS digital integrated Circuits", McGraw-Hill International Edition, Pg No. 357.
[6]. Tanay Karnik, Peter Hazucha and Jagdish Patel, "Single Event Upsets in CMOS Processes" , IEEE Transactions on Dependable and Secure Computing, VOL. 1, NO. 2, April-June 2004
[7]. Robert C. Baumann, "Radiation-Induced Soft Errors in Advanced Semiconductor Technologies" , IEEE Transactions on Device and Material Reliability, VOL. 5, NO. 3, September 2005
[8]. Neil H. E. Weste and Kamran Eshraghian "Principles of CMOS VLSI design,"Addison Wesley, 1994.
[9]. Robert C. Baumann, "Radiation-Induced Soft Errors in Advanced Semiconductor Technologies" , IEEE Transactions on Device and Material Reliability, VOL. 5, NO. 3, September 2005
[10]. R. Baumann, "Soft errors in advanced computer systems," IEEE Trans. Device Mater. Rel., vol. 22, no. 3, pp. 258–266, May-Jun. 2005.